Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An integrated circuit device, comprising

a read only memory matrix, comprising cells organized in columns with associated bit lines and rows with associated word lines, the matrix comprising data transistors coupled to both the bit lines and the word lines in data dependent ones of the cells;

a differential sense amplifier having a first input, a second input, and a control input for controlling activation and deactivation of amplification by the sense amplifier;

a coupling circuit coupled between the bit lines and the first input, for controllably permitting charge sharing between a selectable one of the bit lines and the first input;

a reference circuit coupled to the second input and arranged to controllably activate driving of a reference voltage at the second input;

a timing circuit arranged to signal operation in a first phase, when the word lines have selected a row of the matrix, followed by a second phase, the timing circuit controlling the coupling circuit to permit charge sharing between the input and the selectable one of the bit lines in the first phase, and the timing circuit in the second phase controlling the coupling circuit to prevent said charge sharing, making the reference circuit deactivate driving the reference voltage, and activating amplification by the differential sense amplifier only when said charge sharing has been prevented and said driving has been deactivated.

2. (currently amended) An integrated circuit device according to claim 1, wherein the timing circuit comprises

a dummy bit line capacitively loaded substantially as capacitive loading of a hypothetical bit line with a maximum number of data transistors coupled to that

hypothetical bit line;

a dummy data transistor coupled to the dummy bit line;

a trigger circuit for triggering the second phase, the trigger circuit activating the dummy data transistor in the first phase and starting the second phase when a potential swing on the dummy bit line due to activation of the dummy data transistor in the first phase exceeds a threshold value larger than a potential swing that is needed on the bit line to cross the reference voltage.

3. (canceled)

4. (currently amended) An integrated circuit device according to claim 1, wherein the differential sense amplifier is connected between a first and second power supply connection, the sense amplifier comprising a ~~s~~ first and second switching circuit coupled between the sense amplifier and the first and second power supply connection respectively, the timing circuit deactivating and activating amplification by the sense amplifier by making both switching circuits non-conductive and conductive respectively.

5. (currently amended) An integrated circuit device according to claim 4, wherein the differential sense amplifier comprises a pair of inverters, with inputs coupled to the first and second input respectively and outputs cross coupled to each others inputs, the inverters receiving power supply from the power supply connections via the first and second switching circuit.

6. (currently amended) An integrated circuit device according to claim 5, comprising a latch circuit having inputs coupled to the outputs of the inverters.

7. (original) An integrated circuit device according to claim 1, wherein the reference circuit comprises a controllable equalization circuit coupled between the first and second input and arranged to equalize potentials on said first and second input prior to said first phase.

8. (original) An integrated circuit device according to claim 1, wherein the reference circuit comprises a PMOS bias transistor and an NMOS bias transistor with a main current channel coupled from the second input to a negative and a positive power supply terminal respectively, the timing circuit being arranged to drive the control electrodes of the PMOS bias transistor and the NMOS bias transistor to the potential of the negative and positive power supply terminal respectively during said first phase.

9. (currently amended) An integrated circuit device according to claim 1, wherein the reference circuit comprises an first bias transistor and a second bias transistor of mutually opposite polarity with a main current channel coupled to respective power supply terminals, the timing circuit being arranged to switch the main current channel of the first bias transistor to a conductive state and to switch the second bias transistor as a diode during said first phase.

10. (currently amended) An integrated circuit device according to claim 1, wherein the timing circuit comprises

a dummy bit line with a capacitive load substantially corresponding to a maximum possible capacitive load for any of the bit lines;

a pull transistor for pulling the potential of the dummy bit line starting from a the start of the first phase;

a trigger circuit for triggering the second phase when the potential swing due to said pulling exceeds a threshold value larger than a potential swing that is needed on the bit line to cross the reference voltage.

11. (original) An integrated circuit device according to claim 1, comprising a precharge circuit arranged to precharge the bit lines from a first power supply connection prior to said first phase and to decouple the bit lines from the first power supply connections during said second phase.

12. (currently amended) A method of reading data from a read only memory matrix in an integrated circuit device, the read only memory matrix comprising cells organized in

columns with associated bit lines and rows with associated word lines, the matrix comprising data transistors coupled to both the bit lines and the word lines in data dependent ones of the cells;

providing a differential sense amplifier having a first input a second input and a control input for controlling activation and deactivation of amplification by the sense amplifier;

providing a coupling circuit coupled between the bit lines and the first input for controllably permitting charge sharing between a selectable one of the bit lines and the first input;

providing a reference circuit coupled to the second input the method comprising the following steps:

controllably activating the reference circuit to drive a reference voltage at the second input;

signalling operation in a first phase, when the word lines have selected a row of the matrix, wherein the coupling circuit is controlled to permit charge sharing between the input and the selectable one of the bit lines, followed by a second phase, wherein the coupling circuit is controlled to prevent said charge sharing, making the reference circuit deactivate driving the reference voltage, and activating amplification by the differential sense amplifier only when said charge sharing has been prevented and said driving has been deactivated.

13. (new) The method of claim 12, further comprising a timing circuit having:

a dummy bit line capacitively loaded substantially as capacitive loading of a hypothetical bit line with a maximum number of data transistors coupled to that hypothetical bit line

a dummy data transistor coupled to the dummy bit line

a trigger circuit for triggering the second phase, the trigger circuit activating the dummy data transistor in the first phase and starting the second phase when a potential swing on the dummy bit line due to activation of the dummy data transistor in the first phase exceeds a threshold value larger than a potential swing that is needed on the bit line to cross the reference voltage.

14. (new) The method of claim 12, wherein the reference circuit is local to a periphery of the memory matrix without containing signal lines that extend in parallel with the bit lines over a column height of the matrix.

15. (new) The method of claim 12, wherein the differential sense amplifier is connected between a first and second power supply connection, the sense amplifier comprising a first and second switching circuit coupled between the sense amplifier and the first and second power supply connection respectively, a timing circuit deactivating and activating amplification by the sense amplifier by making both switching circuits non-conductive and conductive respectively.

16. (new) The method of claim 12, wherein the reference circuit comprises a first bias transistor and a second bias transistor of mutually opposite polarity with a main current channel coupled to respective power supply terminals the timing circuit being arranged to switch the main current channel of the first bias transistor to a conductive state and to switch the second bias transistor as a diode during said first phase.

17. (new) The method of claim 12, further comprising a timing circuit having:

a dummy bit line with a capacitive load substantially corresponding to a maximum possible capacitive load for any of the bit lines

a pull transistor for pulling the potential of the dummy bit line starting from a the start of the first phase;

a trigger circuit for triggering the second phase when the potential swing due to said pulling exceeds a threshold value larger than a potential swing that is needed on the bit line to cross the reference voltage.

18. (new) The method of claim 12, wherein the reference circuit comprises a controllable equalization circuit coupled between the first and second input and arranged to equalize potentials on said first and second input prior to said first phase.

19. (new) The method of claim 12, wherein the reference circuit comprises a PMOS bias transistor and an NMOS bias transistor with a main current channel coupled from the second input to a negative and a positive power supply terminal respectively, the timing circuit being arranged to drive the control electrodes of the PMOS bias transistor and the NMOS bias transistor to the potential of the negative and positive power supply terminal respectively during said first phase.

20. (new) An integrated circuit device, comprising:

a read only memory matrix, comprising cells organized in columns with associated bit lines and rows with associated word lines, the matrix comprising data transistors coupled to both the bit lines and the word lines in data dependent ones of the cells;

a differential sense amplifier, having a first input, a second input, and a control input for controlling activation and deactivation of amplification by the sense amplifier;

a coupling circuit coupled between the bit lines and the first input, for controllably permitting charge sharing between a selectable one of the bit lines and the first input;

a reference circuit coupled to the second input, and arranged to controllably activate driving of a reference voltage at the second input;

a timing circuit arranged to signal operation in a first phase, when the word lines have selected a row of the matrix, followed by a second phase, the timing circuit controlling the coupling circuit to permit charge sharing between the input and the selectable one of the bit lines in the first phase, and the timing circuit in the second phase controlling the coupling circuit to prevent said charge sharing, making the reference circuit deactivate driving the reference voltage, and activating amplification by the differential sense amplifier only when said charge sharing has been prevented and said driving has been deactivated;

wherein the reference circuit is local to a periphery of the memory matrix without containing signal lines that extend in parallel with the bit lines over a column height of the matrix.